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Nusym Debuts with Focus on Intelligent Verification

LOS GATOS, Calif., May 14, 2008 -- Nusym Technology, Inc. formally introduced itself today as a verification solutions provider targeting one of the most critical problems in electronic design: developing confidence in the design in a fraction of the time and resources of current methods. Nusym is focused on an “Intelligent Verification” approach that leverages design insight to automatically drive rapid verification closure.

The company has raised \$8 million of capital to date. Nusym’s investment funding comes from premiere firms such as Woodside Funds, Draper Richards, L.P., as well as prominent EDA veterans, including Lucio Lanza and John Sanguinetti.

“With current verification methods, it is possible to get 70-80% coverage but it takes an enormous investment of time and resources to improve beyond that,” stated Venkatesh Shukla, President and CEO of Nusym. “This problem has been well understood for over a decade but attempts to solve it thus far have fallen short. This is where Nusym is focused – how to improve coverage automatically.”

Nusym’s technology is currently being evaluated on a number of leading edge designs at its semiconductor partners. Nusym will announce its flagship product at a later date.

“We find Nusym to have a very promising verification technology. It can run on very large design blocks and target hard to hit coverage points”, said Dan Smith, Director of CAD for NVIDIA.

Importance of Intelligent Verification

The size and complexity of modern Integrated Circuits (ICs) dictate an extensive verification phase to ensure correct functionality prior to fabrication. Today there is no way to ascertain whether a design has been fully verified with 100% confidence, elevating the risk of undiscovered faults, or bugs, in the final product. Incorrect device operation not discovered during this process often results in a fabrication re-spin, driving extensive cost and schedule overruns.

In the 1990’s, verification was performed by IC designers who manually tested their code with an understanding of its structure. With the increase in chip size, these manual verification methodologies became unwieldy and the industry transitioned to a more efficient test generation model. Verification approaches such as constrained random verification, which treats the design as “black box” and randomly generates test vectors with no correlation between inputs and coverage points, enabled good coverage relatively quickly. However, achieving coverage closure

with a constrained random approach is becoming nearly impossible despite huge time and resource investments due to its open loop nature.

Formal and semi-formal approaches applied a more “intelligent” verification style, leveraging design internals to improve effectiveness. However, their use on full designs has been impractical due to severe capacity limitations and their inability to leverage current testbench infrastructure.

An ideal, “Intelligent Verification” approach would be able to use existing testbenches, along with the design, and automatically determine how to maximize coverage. At the same time it would be able to direct the user to reasons why certain coverage points were not being detected. Such an approach would avoid the unnecessary random wandering of constrained random test methods to find a bug; instead it would automatically track efficient traces through the design to coverage points. Requiring “white box” analysis of the design and testbench, intelligent verification would also ensure that no simulation cycles are wasted in verifying items that have already been tested.

Nusym Company Focus

Nusym will provide intelligent verification solutions that address the following key challenges in electronic design today: increasing verification confidence; tracking hard to reach design areas; and eliminating test redundancy, utilizing an automated, simulation-based method which scales to large designs and requires minimal change in current verification methodologies.

Unlike current methods which either treat the design as a “blackbox”, or are impractical for use on large designs, Nusym will focus on a uniquely intelligent approach that, like a designer, uses insight into the design to create “directed” tests automatically.

“Nusym has the most exciting technological approach to functional verification that I have seen in a long time,” said John Sanguinetti, Nusym board member and Forte Design Systems founder and CTO. “The founders’ backgrounds in hardware design and verification give them a practical perspective that blends deep understanding of end user verification challenges with breakthrough algorithms and heuristics.”

Nusym will be holding suite demonstrations of its technology for potential users at the Design Automation Conference (DAC) in Anaheim, California from June 8th to 13th, at suite number 379. To request a suite demonstration, please visit the Nusym website: www.nusym.com.

Nusym Management Team

Venktesh Shukla: President and CEO, was senior vice president of marketing and business development at Magma Design Automation Inc prior to joining Nusym. Before joining Magma, Shukla was CEO of Everypath, a leader in enterprise mobile computing. Mr. Shukla also held executive positions at Ambit and Cadence Design Systems. Mr. Shukla helped found the standards organization Open Verilog International (OVI), which has since become Accellera. He holds a Masters in Management from MIT Sloan School of Management and a Bachelors of Electronics from M.A. National Institute of Technology, Bhopal in India.

Dr. Chris Wilson: Founder and CTO, worked at Amdahl, Andor Systems, Tandem Computers, HaL Computers, and Candlestick Networks. Mr. Wilson led hardware development efforts spanning architecture definition to design, verification, and bring up. Chris received a Ph.D. in Electrical Engineering from Stanford University in 2002. He received a MS in EE from Stanford and BS in Computer and Systems Engineering from Rensselaer Polytechnic Institute.

Jayant Nagda: Vice President of Engineering, was group director R&D in VCS group at Synopsys Inc. where he was responsible for verification technologies such as assertions, coverage, test bench automation and formal technologies. Previously Jayant was founder and CEO of CADWorx Consulting Inc, which provided consulting services for chip design, verification and EDA software development. Prior to CADWorx, Mr. Nagda was at Cadence Design Systems, involved with synthesis and simulation. Jayant received a Masters degree in Computer Engineering from Indian Institute of Technology, Delhi and a Bachelor of Engineering degree from Bombay University.

Raghu Srigiriraju: Vice President and Managing Director, Nusym Technology India Pvt Ltd., had been founder and CEO of EDA software services company, Mirafra Technologies. Prior to this, Srigiriraju led major R&D efforts for VCS at Synopsys. Mr. Srigiriraju received a Bachelor's degree in Electrical Engineering from Indian Institute of Technology, Madras and a Masters in Computer Engineering from the University of Massachusetts, Amherst.

About Nusym

Nusym Technology, Inc. is focused on delivering rapid verification closure solutions that allow design teams to automatically leverage insight into the design structure, intelligently driving the verification process to increase confidence and efficiency. Nusym is backed by top-tier venture investors that include Woodside Fund and Draper Richards, LP. The company is headquartered at 420 Blossom Hill Road, Suite 201, Los Gatos, Calif. 95032. For more information, please visit the company's website at www.nusym.com or visit us at DAC during June 8-13 at suite number 379.

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